Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 1, 2 and 4-24 are pending in the application, with claims 1 and 8 being the independent claims. Claims 1, 6-9, 11-13, 15-19 and 21 are sought to be amended. Claim 3 is sought to be cancelled without prejudice to or disclaimer of the subject matter therein. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Objection to the Specification

The Examiner has objected to the text at page 20, lines 29-30 of the specification for improperly characterizing FIG. 4 as a flow chart rather than an apparatus. The Examiner has also objected to the text at page 20, line 37 and page 21, lines 5 and 7 for referring to element 6 of FIG. 4 as a "de-multiplexer" rather than a "multiplexer". Applicants have amended the specification to address these issues identified by the Examiner. Accordingly, Applicants respectfully request that the objection to the specification be reconsidered and withdrawn.

Objections to the Drawings

The Examiner has objected to FIG. 4 as being a "hand drawn drawing with typed words." In response, Applicants submit herewith a replacement drawing sheet that

includes a formal drawing for FIG. 4. Accordingly, Applicants respectfully request that the objection to the drawings be reconsidered and withdrawn.

Rejections under 35 U.S.C. § 112

The Examiner has rejected claims 3 and 6-20 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as their invention. Claim 3 has been cancelled, thereby rendering the rejection of that claim moot. Claims 6-19 and 21 have been amended to address the issues set forth by the Examiner in support of these rejections, with the exception of those issues set forth below.

With respect to claim 9, Applicants respectfully disagree with the Examiner's assertion that there is insufficient antecedent basis for the claim term "the instruction fetch" in line 3 of claim 9 as originally filed, since line 2 of claim 9 as originally filed includes the term "an instruction fetch".

With respect to claim 18, Applicants respectfully disagree with the Examiner's assertion that there is insufficient antecedent basis for the claim term "the interrupt request" in lines 3-4 of claim 18 as originally filed, since line 2 of claim 18 as originally filed includes the term "an interrupt request".

With respect to claim 19, Applicants respectfully disagree with the Examiner's assertion that there is insufficient antecedent basis for the claim term "the interrupt request" in lines 3-4 of claim 19 as originally filed, since line 2 of claim 19 as originally filed includes the term "an interrupt request." With further respect to claim 19, Applicants respectfully disagree with the Examiner's assertion that there is insufficient

antecedent basis for the claim term "the instruction fetch stage" in line 5 of claim 19 as originally filed, since claim 16 upon which claim 19 depends recites "an instruction fetch stage."

It has been assumed by Applicants that the rejection of claim 20 under 35 U.S.C. § 112 for providing insufficient antecedent basis for the claim term "the co-processor" was actually directed to claim 21. Applicants have addressed this issue by changing the dependency of claim 21.

In view of the foregoing, Applicants respectfully request that the rejection of claims 3 and 6-20 under 35 U.S.C. § 112, second paragraph, be reconsidered and withdrawn.

Rejections under 35 U.S.C. § 102

The Examiner has rejected claims 1-3, 5-7 and 24 under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 4,777,587 to Case *et al.* ("Case"). Based on the foregoing amendments and for the reasons set forth below, Applicants respectfully traverse.

Independent claim 1, as presently amended, is directed to a method of processing an interrupt verification support mechanism in a computer system that includes a processor and an input for external interrupts communicatively coupled to the processor. The method includes the steps of:

> (a) processing at least one actual instruction in the processor; and
>
> (b) if an external interrupt request or an interrupt pseudo-instruction is received by the processor, replacing the actual instruction in an instruction fetch stage of the processor with the pseudo-instruction.

Case does not teach or suggest each and every feature of independent claim 1 as presently amended. For example, as will be explained in more detail below, Case does not teach or suggest "replacing [an] actual instruction in an instruction fetch stage of the processor with [a] pseudo-instruction" as recited by claim 1.

Case is directed to an instruction processor suitable for use in a reduced instruction set computer (RISC) that executes a branch instruction in a single cycle and in a manner that does not disrupt the instruction pipeline. Case's instruction processor achieves this, in part, by using special hardware to fetch the instruction at a branch target address during execution of the branch instruction. As a result, the instruction to which the branch passes control (the "target instruction"), enters the pipeline two stages behind the branch instruction. A "branch delay instruction" always immediately follows the branch instruction and precedes the target instruction in the pipeline such that the instruction pipeline is not disrupted:

> As shown in FIG. 2, a branch delay instruction "DELAY" physically follows the branch instruction and is always executed; the branch itself not occurring until after the branch delay instruction, whereupon the instruction to which the branch instruction passes control "TARGET" executes. In this manner, the processor 10 can always fetch the next instruction during the execution of the current instruction, i.e., operate in a pipeline mode without the need to interrupt the pipeline nor retract the fetching of an instruction.

Case, column 4, lines 31-40. Also, since the "branch delay instruction" always follows the branch instruction in the pipeline, there is no need to replace the instruction that normally would follow the branch instruction:

> An instruction calling for a branch will be processed by processor 10 so that the branch does not occur until the instruction following the branch instruction is executed. In this manner, the instruction pipeline, implemented by the PC stack pipeline 32, operates without interruption even when a branch instruction enters the pipeline, *since no replacement*

> *of the instruction which normally follows the branch instruction need be made in the pipelin*e.

Case at column 3, lines 52-55 (emphasis added).

Thus, Case makes clear that one instruction is *never* replaced by another at any stage of Case's instruction pipeline.[1] In contrast, claim 1 as presently amended includes the feature of "replacing [an] actual instruction in an instruction fetch stage of the processor with [an] pseudo-instruction." A specific implementation of this feature is shown in FIG. 4 and described at page 21, lines 16-18, of the specification of the present application, which states: "When the program counter PC matches the interrupt register, or an external interrupt is present, the actual instruction [fetched by an instruction fetch stage 1] is replaced with a pseudo-instruction."

Since independent claim 1 as presently amended includes the feature of replacing an actual instruction in an instruction fetch stage with a pseudo-instruction, and Case teaches never replacing instructions at any stage of an instruction pipeline, Case cannot anticipate independent claim 1. Dependent claims 2, 5-7 and 24 are likewise not anticipated by Case for the same reasons as independent claim 1 from which they depend and further in view of their own respective features. Dependent claim 3 has been cancelled. Accordingly, Applicants respectfully request that the rejection of claims 1-3, 5-7 and 24 under 35 U.S.C. § 102(b) be reconsidered and withdrawn.

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[1] In formulating the rejection, the Examiner refers to text at column 5, line 24 to column 6, line 44 of Case (and associated FIGS. 3A and 3B) which describes special-handling techniques for calls on subroutines, interrupts and trap routines used by Case's instruction processor. While this text describes aborting instructions in the instruction pipeline, it does not describing replacing instructions with other instructions in any stage of the instruction pipeline.

Rejections under 35 U.S.C. § 103

Claim 4

The Examiner has rejected dependent claim 4 under 35 U.S.C. § 103(a) as being unpatentable over Case as applied to independent claim 1 in view of U.S. Patent No. 4,498,136 to Sproul, III ("Sproul"). As described above, Case does not teach or suggest each and every feature of independent claim 1. Sproul does not provide the missing teachings or suggestions with respect to claim 1. Conseqently, the combination of Case and Sproul cannot render obvious independent claim 1. Dependent claim 4 is likewise not rendered obvious by the combination of Case and Sproul for the same reasons as independent claim 1 from which it depends and further in view of its own respective features. Accordingly, Applicants respectfully request that the rejection of claim 4 under 35 U.S.C. § 103(a) be reconsidered and withdrawn.

Claims 8-23

The Examiner has rejected claims 8-23 under 35 U.S.C. § 103(a) over Case in view of Sproul. Based on the foregoing amendments and for the reasons set forth below, Applicants respectfully traverse.

Independent claim 8, as presently amended, is directed to an interrupt verification support mechanism device for a computer system comprising a processor and an input for external interrupt requests or interrupt pseudo-instructions communicatively coupled to the processor. The device includes:

> a set of one or more interrupt registers each of which contains information, the information including at least a program counter of the instruction which is to be interrupted and a sort of interrupt to use, so as to enable the device to process at least one actual instruction, and if an external interrupt request is received by the processor, the at least one actual instruction is replaced with the pseudo-instruction.

Case does not teach each and every feature of independent claim 8 as presently amended. For example, as will be explained in more detail below, Case does not teach or suggest "one or more interrupt registers" each of which includes "a program counter of [an] instruction which is to be interrupted."

As discussed above with respect to claim 1, Case is directed to an instruction processor suitable for use in a reduced instruction set computer (RISC) that executes a branch instruction in a single cycle and in a manner that does not disrupt the instruction pipeline. Case discusses interrupts only in the context of describing special-handling techniques that must be used for interrupts that occur between a branch instruction and a "branch delay instruction." *See* Case, column 5, line 24-column 6, line 44. However, this section describes only how interrupts are handled and is completely silent with respect to how interrupts are caused or how instructions to be interrupted are identified. Thus, this section clearly does not describe "one or more interrupt registers" each of which includes "a program counter of [an] instruction which is to be interrupted" as recited by claim 8.

Sproul does not in any way rectify this deficiency of Case with respect to independent claim 8. Consequently, the combination of Case and Sproul does not render claim 8 obvious. Dependent claims 9-23 are likewise not rendered obvious by the combination of Case and Sproul for the same reasons as independent claim 8 from which they depend and further in view of their own respective features. Accordingly, Applicants respectfully request that the rejection of claims 8-23 under 35 U.S.C. § 103(a) be reconsidered and withdrawn.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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